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EXAMINER	
PETRANEK, JACOB ANDREW	
ART UNIT	**PAPER NUMBER**
2183	

NOTIFICATION DATE	DELIVERY MODE
03/21/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/538,369	BURNS ET AL.	
	Examiner	Art Unit	
	JACOB PETRANEK	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,11-18 and 20-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,11-18 and 20-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-8, 11-18, 20-23 are pending.

2. In view of the appeal brief filed on 1/7/2008, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitations of claim 1 "coprocessor coupled to a main processor" and "interface module" must be shown or the feature(s) canceled from the claim(s). This can be corrected in figure 1 by filling in the boxes to show which element is the coprocessor, main processor, and interface module. Also, claims 11-12, and 14 are not shown in the drawings. Claims related to figure 4 are also objected to because the figure contains no information that states what each box represents. No new matter should be entered. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d).

Claim Objections

4. Claim 1 is objected to because of the following informalities:

5. Claim 1 line 1 recites "a coprocessor to a main processor …" that should be changed to "a coprocessor coupled to a main processor …"

New Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 3, 5-8, 12-13, 15-16, and 20-23 are rejected under 35 U.S.C. §103(a) as being unpatentable over Fleck et al. (U.S. 6,434,689), in view of Roussakov (U.S. 6,092,174).

8. As per claim 1:

Fleck disclosed a coprocessor to a main processor having an execution speed greater than that of said processor, the coprocessor comprising:

Being communicatively connected to said processor by an interface module (Fleck: Figure 1 elements 7 and 4c, column 3 lines 19-28)(Figure 1 shows a coprocessor connected to a processor via interface element 7. The elements above the interface are the processor.)

Fleck failed to teach a two-dimensional array of processing cells and having a mechanism for reconfiguring a plurality of information paths between the interface module and respective cells on a periphery of the array.

However, Roussakov disclosed a two-dimensional array of processing cells (Roussakov: Figure 1 element 1, column 5 lines 20-33) and having a mechanism for reconfiguring a plurality of information paths between the interface module and respective cells on a periphery of the array (Roussakov: Figure 3 elements 17 and 18, column 7 lines 1-24)(The limitations broadest reasonable interpretation is reconfiguring a plurality of information paths between the processing cells and the interface module. The FPGA allows for reconfigurations of data paths between the microcomputer modules, which are between the processing cells and the interface. The data paths transmit information and are therefore considered information paths.).

Fleck disclosed using a FPGA as part of the coprocessor of the system, but failed to disclose the details of the FPGA. Fleck also disclosed that the advantage of using FPGA's allows for benefits from being able to re-program them to perform specific tasks (Fleck: Column 4 lines 18-40). One of ordinary skill in the art would have been motivated by the lack of information by Fleck on FPGA's to add the functionality of Roussakov. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the FPGA of Roussakov into the processor of Fleck for the advantage of detailing the functionality of the FPGA of Fleck.

9. As per claim 3:

Fleck and Roussakov disclosed the paths are connected one-to-one with said respective cells (Roussakov: Figure 5 element 1)(Figure 5 shows that connections between the microcomputer clusters are between the same column and row of a microcomputer cluster.).

10. As per claim 5:

Fleck and Roussakov disclosed inter-cell connection within the array is such that each cell of the array is connected only to cells whose column is the same and whose row is immediately adjacent, and only to cells whose row is the same and whose column is immediately adjacent (Roussakov: Figure 5 element 1)(Figure 5 shows that connections between the microcomputer clusters are between the same column and row of a microcomputer cluster.).

11. As per claim 6:

Fleck and Roussakov disclosed the coprocessor of claim 1, wherein the coprocessor interface module and main processor of claim 1 and a shared memory that communicatively connects with the interface module and the main processor to provide the main processor to coprocessor connection (Fleck: Figure 1 element 5, column 2 lines 56-58)(Official notice is given that an instruction fetch unit fetches instructions from a memory. Thus, it's obvious to one of ordinary skill in the art that there's a memory coupled to the instruction fetch unit. This memory not shown in figure 1 is shared and provides instructions for both the main processor and the coprocessor.).

12. As per claim 7:

Fleck and Roussakov disclosed the coprocessor of claim 1, including an array processor that comprises said two-dimensional array (Roussakov: Figure 1 element 1, column 5 lines 20-33).

13. As per claim 8:

Claim 8 essentially recites the same limitations of claim 1. Therefore, claim 8 is rejected for the same reasons as claim 1.

14. As per claim 12:

Fleck and Roussakov disclosed the coprocessor of claim 1, wherein said processor comprises a general purpose processor (Fleck: Figure 1, column 2 lines 34-47)(Processors are inherently considered general-purposes unless otherwise explicitly stated.).

15. As per claim 13:

Fleck disclosed a functional unit serving as a component of a main processor (Fleck: Figure 1 elements 7 and 4c, column 3 lines 19-28)(Figure 1 shows a coprocessor connected to a processor via interface element 7. The elements above the interface are the main processor. The coprocessor is the functional unit.)

Fleck failed to teach a functional unit having a two-dimensional array of processing cells, the unit having a mechanism for reconfiguring a plurality of intra-processor information paths to the array to respective cells on a periphery of the array.

However, Roussakov disclosed a functional unit having a two-dimensional array of processing cells (Roussakov: Figure 1 element 1, column 5 lines 20-33), the unit having a mechanism for reconfiguring a plurality of intra-processor information paths to the array to respective cells on a periphery of the array (Roussakov: Figure 3 elements 17 and 18, column 7 lines 1-24)(The limitations broadest reasonable interpretation is reconfiguring a plurality of information paths within the processing cells. The FPGA allows for reconfigurations of data paths within the microcomputer modules, which are the processing cells. The data paths transmit information and are therefore considered information paths.).

Fleck disclosed using a FPGA as part of the coprocessor of the system, but failed to disclose the details of the FPGA. Fleck also disclosed that the advantage of using FPGA's allows for benefits from being able to re-program them to perform specific tasks (Fleck: Column 4 lines 18-40). One of ordinary skill in the art would have been motivated by the lack of information by Fleck on FPGA's to add the functionality of Roussakov. Thus, it would have been obvious to one of ordinary skill in the art at the

time of the invention to implement the FPGA of Roussakov into the processor of Fleck for the advantage of detailing the functionality of the FPGA of Fleck.

16. As per claim 15:

The additional limitation(s) of claim 15 basically recite the additional limitation(s) of claim 5. Therefore, claim 15 is rejected for the same reason(s) as claim 5.

17. As per claim 16:

Fleck and Roussakov disclosed the unit of claim 13, further including means for transmitting a plurality of array programs to corresponding predetermined subsets of said processing cells (Roussakov: Figure 5 element 9, column 9 lines 41-50)(The pathway batch controller sends data to the microcomputer clusters to execute.).

18. As per claim 20:

Claim 20 essentially recites the same limitations of claim 1. Claim 20 additionally recites the following limitations:

The coprocessor has a execution speed greater than the processor (Roussakov: Column 3 lines 3-7)(The FPGA is able to be optimized to perform computer operations and is faster than computer processors. The processor of Fleck is considered one of the computer processors mentioned by Roussakov and thus is slower than the FPGA.).

19. As per claim 21:

Fleck and Roussakov disclosed the coprocessor of claim 1, wherein the array is rectangular (Roussakov: Figure 1, column 5 lines 34-40)(The array of microcomputer clusters is square shaped. However, Roussakov states the array size can be expanded. It's obvious to one of ordinary skill in the art that expanding the array can

result in a rectangular shape.), wherein the periphery consists of those of said processing cells located in all of a first row, last row, first column and last column of said array (Periphery by definition is the boundary of an area (The American Heritage Dictionary of the English Language, Fourth Edition), therefore the periphery of the array is inherently the first row, last row, first column and last column.), and wherein the interface module's mechanism for reconfiguring a plurality of information paths reconfigures information paths directly connecting the interface module and each of the cells on the periphery of the array (Roussakov: Figure 3 elements 17 and 18, column 7 lines 1-24)(The FPGA allows for reconfigurations of data paths between the microcomputer modules, which are between the processing cells and the interface. The data paths transmit information and are therefore considered information paths.).

20. As per claim 22:

Fleck and Roussakov disclosed the coprocessor of claim 1, wherein the interface comprises a plurality of border cells directly connected to the respective processing cells on the periphery of the array (Roussakov: Figure 1)(The border cells of figure 1 are connected to other border cells of the array.).

21. As per claim 23:

Fleck and Roussakov disclosed the coprocessor of claim 1, further comprising a master cell for forwarding array programs to the processing cells of the two-dimensional array (Roussakov: Figure 5 element 9, column 9 lines 41-50)(The pathway batch controller sends data to the microcomputer clusters to execute. Element 9 is the master cell that sends data to the individual microcomputer clusters.).

22. Claim 2 is rejected under 35 U.S.C. §103(a) as being unpatentable over Fleck et al. (U.S. 6,434,689), in view of Roussakov (U.S. 6,092,174), further in view of Miyamori et al. ("REMARC: Reconfigurable multimedia array coprocessor").

23. As per claim 2:

Fleck and Roussakov disclosed the coprocessor of claim 1.

Fleck and Roussakov failed to teach the array comprises a systolic processing array.

However, Miyamori discloses the array comprises a systolic processing array (Miyamori: Figure 2, page 396 column 1 paragraph 2).

The advantage of arranging a reconfigurable architecture in a systolic manner is that it can exploit fine-grained parallelism and achieve higher performance versus other multimedia extensions (Miyamori: Page 389 column 2 paragraph 2). One of ordinary skill in the art would have been motivated by this advantage to allow for systolic processing on the processing array of Roussakov. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement systolic processing on the array of Roussakov to gain increased performance by exploiting fine-grained parallelism.

24. Claim 11 is rejected under 35 U.S.C. §103(a) as being unpatentable over Fleck et al. (U.S. 6,434,689), in view of Roussakov (U.S. 6,092,174), further in view of Taylor (U.S. 5,857,109).

25. As per claim 11:

Fleck and Roussakov disclosed the coprocessor of claim 1.

Fleck and Roussakov failed to teach processor wherein said processor comprises a digital signal processor.

However, Taylor disclosed wherein said processor comprises a digital signal processor (Taylor: Figure 42, column 5 lines 23-26).

The advantage of DSP's is that they enhance video output processing (Taylor: abstract). One of ordinary skill in the art would have been motivated by this advantage to implement the general-purpose processor of Fleck as a DSP. Thus, one of ordinary skill in the art at the time of the invention would have implemented the general-purpose processor of Fleck as a DSP for the advantage of enhanced video output processing.

26. Claims 4, 14, and 17-18 are rejected under 35 U.S.C. §103(a) as being unpatentable Fleck et al. (U.S. 6,434,689), in view of Roussakov (U.S. 6,092,174), further in view of Barat et al. ("Reconfigurable instruction set processor: An implementation platform for interactive multimedia applications").

27. As per claim 4:

Fleck and Roussakov disclosed the coprocessor of claim 1.

Fleck and Roussakov failed to teach wherein the coprocessor performs mathematical operations whose timing is based on a flow of input operands along the paths.

However, Barat disclosed wherein the coprocessor performs mathematical operations whose timing is based on a flow of input operands along the paths (Barat: Page 484 column 1 paragraph 2)(The compiler generates code with timing delays of the processing elements and interconnects in mind. Official notice is given that instructions executed on a processor can include mathematical operations that use operands. Thus, it's obvious to one of ordinary skill in the art that the instructions executed are mathematical operations that use operands.).

The advantage of the reconfiguration method of Barat is that it allows for a compiler to more efficiently execute loops by storing configurations locally (Barat: Page 483, section 2.2 paragraph 2). One of ordinary skill in the art would have been motivated by this advantage to implement it within the processor of Roussakov. Thus, one of ordinary skill in the art at the time of the invention would have implemented the reconfiguration method of Barat into the processor of Roussakov for the advantage of more efficiently executing loops.

28. As per claim 14:

Fleck and Roussakov disclosed the coprocessor of claim 13.

Fleck and Roussakov failed to teach wherein said processor comprises a very long instruction word (VLIW) processor.

However, Barat discloses processor comprises a very long instruction word (VLIW) processor (Barat: Page 482 column 2 paragraph 2).

The advantage of VLIW processors is that they reduce the execution time of interactive multimedia applications (Barat: Page 485 column 1 paragraph 2). One of

ordinary skill in the art would have been motivated by this to implement the general-purpose processor of Fleck as a VLIW processor. Thus, one of ordinary skill in the art at the time of the invention would have implemented the general-purpose processor of Fleck as a VLIW for the advantage of reducing the execution time of interactive multimedia applications.

29. As per claim 17:

Fleck and Roussakov disclosed a system including the processor of claim 16.

Fleck and Roussakov failed to teach an array program generator for generating the array programs to be transmitted, and, when needed, updating a program, transmitting the updated program, and transmitting concurrently, when needed, a reconfigure signal to said mechanism to correspondingly update a current steady state connection pattern of said information paths.

However, Barat disclosed an array program generator for generating the array programs to be transmitted (Barat: Page 483, section 2.2 paragraph 2)(The compiler generates programs executed on the array of Roussakov.), and, when needed, updating a program, transmitting the updated program, and transmitting concurrently, when needed, a reconfigure signal to said mechanism to correspondingly update a current steady state connection pattern of said information paths (Barat: Page 483, section 2.2 paragraph 1)(The ROP field will be a signal to update the reconfigurable microcomputer clusters of Roussakov to be able to execute an instruction. The instruction that is executed is also transferred to the array to be executed.).

The advantage of the reconfiguration method of Barat is that it allows for a compiler to more efficiently execute loops by storing configurations locally (Barat: Page 483, section 2.2 paragraph 2). One of ordinary skill in the art would have been motivated by this advantage to implement it within the processor of Roussakov. Thus, one of ordinary skill in the art at the time of the invention would have implemented the reconfiguration method of Barat into the processor of Roussakov for the advantage of more efficiently executing loops.

30. As per claim 18:

Fleck, Roussakov, and Barat disclosed the system of claim 17, further including a compiler configured for receiving, in response to said program updating data representative of input and output timing for said unit (timing delay) and further configured for compiling an instruction based on said data (Barat: Page 484 column 1 paragraph 2)(The compiler generates code with timing delays of the processing elements and interconnects in mind.).

Response to Arguments

31. The arguments presented by Applicant in the response, received on 1/7/2008 are considered persuasive.

32. Applicant argues “Callahan disclosed that the Garp array is a two-dimensional array of CLB's interconnected by programmable wiring ... but it certainly does not disclose that the programming wiring "reconfigures a plurality of intra-processor information paths to the array.""

This argument is found to be persuasive for the following reason. The examiner agrees that Callahan doesn't teach reconfiguring a plurality of intra-processor information paths to the array. However, a new ground of rejection has been given to all of the claims. All other arguments based on Callahan are now moot.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Gilson (U.S. 6,622,233), taught an FPGA processor with processing elements.

Cloutier (U.S. 5,892,962), taught an FPGA processor with processing elements connected to a host processor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

Jacob Petranek
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